REMARKS

In this Amendment, Applicants have amended the specification; and amended claim 1 to more appropriately define the present invention.

At the outset, Applicants note that while the Examiner acknowledged Applicants' election of claims 1-6 in response to the Restriction Requirement imposed by the Examiner in the Office Action dated June 25, 2004, the Examiner did not indicate in the present Office Action that non-elected claims 7-14 were withdrawn from further consideration. Applicants assume this was due to an oversight, and therefore assume that claims 7-14 have been withdrawn by the Examiner as being drawn toward a non-elected invention. Claims 1-6 are under current examination.

In the Office Action, the Examiner rejected claims 1, 2, and 5 under 35 U.S.C. § 103(a) as being unpatentable over Chang (U.S. Patent No. 6,737,324); rejected claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Chang in view of Wu (U.S. Patent No. 6,063,680) and Oda (U.S. Patent No. 6,288,430); and rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Chang in view of Kaneshiro et al. (U.S. Patent No. 5,427,964). Applicants respectfully traverse the rejections of claims 1-6, as set forth above, because the Examiner has failed to establish a *prima facie* case of obviousness.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. M.P.E.P. § 2143.

Claim 1 recites a semiconductor device having a MOSFET. The MOSFET comprises, among other things, source and drain regions, a gate insulating film, "a gate electrode which is formed on the gate insulating film and formed of a poly-$Si_{1-x}Ge_x$ layer having a Ge/(Si+Ge) composition ratio x ($0<x<0.2$)," and first, second, and third metal silicide films.

Chang discloses a method of fabricating a raised source/drain of a semiconductor device. Chang at col. 2, lines 5-6. The gate structure of Chang comprises "a thin oxide layer 202 and a conductive layer 204." Col. 3, lines 20-24. Conductive layer 204 "comprises, for example, polysilicon or other suitable conductive materials." Id. at col. 3, lines 21-22 and Fig. 2A. After "an etching process," conductive layer 204 is patterned "into a gate conductive layer 204a." Col. 3, lines 24-27. Gate conductive layer 204a, however, does not include SiGe, and therefore does not correspond to the claimed "gate electrode ... formed of a poly-$Si_{1-x}Ge_x$ layer," as recited in amended claim 1.

Applicants note that Chang discloses an elevated SiGe layer 212 "formed on gate conductive layer 204a" (col. 3, lines 43-45). Elevated SiGe layer 212 is provided as an additional layer "to lower resistance of the gate conductive layer 204a," but is not described as *forming* gate conductive layer 204a itself. Rather, as noted above, gate conductive layer 204a is formed of polysilicon or other suitable conductive materials." Col. 3, lines 21-22 . Chang therefore certainly fails to teach or suggest the claimed "a gate electrode which is formed on the gate insulating film and formed of a poly-$Si_{1-x}Ge_x$ layer," as recited in claim 1 for this reason also.

The Examiner acknowledges that Chang fails to disclose a poly-$Si_{1-x}Ge_x$ layer having a Ge/(Si+Ge) composition ratio x ($0<x<0.2$). Office Action at page 3. The Examiner, however, attempts to cure this deficiency by alleging that "it would have been

obvious ... for the poly-$Si_{1-x}Ge_x$ layer having a Ge/(Si+Ge) composition ratio x ($0<x<0.2$) because it is a used material for the gate electrode." Office Action at page 3. Applicants respectfully disagree.

Determinations of obviousness must be supported by evidence on the record. See *In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001) (finding that the factual determinations central to the issue of patentability, including conclusions of obviousness by the Board, must be supported by "substantial evidence"). In this case, the Office Action provides no "substantial evidence" to support the claimed composition ratio. The Examiner's conclusory statements in the Office Action are not properly supported by facts on the record and do not evidence that one of ordinary skill in the art would have been motivated to form a poly-$Si_{1-x}Ge_x$ layer having a Ge/(Si+Ge) composition ratio x ($0<x<0.2$).

Further, Applicants direct the Examiner's attention to M.P.E.P. § 2143.01, which makes clear that the "mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." As explained above, the Examiner does not show that Chang "suggests the desirability" of the forming a poly-$Si_{1-x}Ge_x$ layer with the claimed composition ratio. No objective reason for modifying the applied art, other than the Examiner's attempt to meet the elements of claim 1, has been established.

Accordingly, Chang fails to teach or suggest "a gate electrode which is formed on the gate insulating film and formed of a poly-$Si_{1-x}Ge_x$ layer," and there is no motivation to form the poly-$Si_{1-x}Ge_x$ layer "having a Ge/(Si+Ge) composition ratio x ($0<x<0.2$)," as recited in claim 1. Applicants therefore submit that independent claim 1 is allowable, for the reasons presented above. Claims 2 and 5 are also allowable at least due to their dependence from claim 1.

On pages 4-5 of the Office Action, the Examiner rejected claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Chang in view of Wu and Oda. Applicants respectfully traverse this rejection as well.

As discussed above, Chang does not teach or suggest each and every element of claim 1, and thus, of claims 3 and 4, which depend therefrom. Wu and Oda fail to cure the above-described deficiencies of Chang. Specifically, Wu, cited merely for the disclosure of metal plugs, and Oda, cited merely for the disclosure of barrier metal layers, are silent as to "a gate electrode which is formed on the gate insulating film and formed of a poly-$Si_{1-x}Ge_x$ layer having a Ge/(Si+Ge) composition ratio x ($0<x<0.2$)," as recited in claim 1. Thus, the applied references, either taken alone or in combination, fail to teach or suggest each and every element of claims 3 and 4, which depend from claim 1. Claims 3 and 4 are therefore allowable at least for this reason.

Applicants respectfully traverse the Examiner's rejection of claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Chang et al. in view of Kaneshiro et al. Office Action at pages 5-6. None of the applied references, either taken alone or in combination, teach or suggest each and every element of claim 6.

Claim 6 depends from claim 1. As discussed above, Chang does not teach or suggest each and every element of claim 1. Kaneshiro et al., cited merely for the disclosure of wells, fails to teach or suggest "a gate electrode which is formed on the gate insulating film and formed of a poly-$Si_{1-x}Ge_x$ layer having a Ge/(Si+Ge) composition ratio x ($0<x<0.2$)," as recited in claim 1. Claim 6 is therefore allowable at least due to its dependence from claim 1.

In view of the foregoing, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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